19.5 A Dual-Band CMOS Transceiver for 3G TD-SCDMA

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Time-division synchronous code-division multiple access (TD-SCDMA) technology, initiated by the China Wireless Telecommunications Standard Group (CWTS), was adopted as one of the 3G standards by International Telecommunication Union (ITU) in 2000. Though the main structure of TD-SCDMA core network is similar to that of WCDMA and CDMA2000, it offers unique features such as asymmetric up/down link, smart antenna, joint detection and baton handover to improve the spectrum efficiency and system capability [1]. In this paper, a dual-band TD-SCDMA RF transceiver compliant to its specifications is reported. This device integrates a VCO, a fractional-N PLL, a receive channel-select filter, and a transmit driver amplifier into a single chip. The transceiver is fabricated in a 0.18μm CMOS process.

The block diagram of the transceiver IC is illustrated in Fig. 19.5.1. Along with an analog baseband (ABB) IC and a digital baseband (DBB) IC, it provides full TD-SCDMA signal processing functions. The ABB IC includes digital signal processing which compensates the analog channel-select filter and performs DC-offset calibration.

The receiver utilizes the direct-conversion architecture, consisting of two LNAs, a double-balanced mixer and I/Q analog filters. Two frequency bands are supported: 1880 to 1920MHz and 2010 to 2025MHz. The LNAs are implemented as fully differential common-source amplifiers with on-chip inductive degeneration. The use of differential topology suppresses the common-mode noise and reduces the sensitivities to the package parasitics. The two LNAs shares the same LC-tank load and degeneration inductor to reduce the area. The LNAs incorporate three voltage gain modes: 20, 0, and –10dB. The low-gain mode is critical to satisfy the maximum input power and adequate dynamic range requirements. The measured LNA noise figure (NF) at its maximum gain is 1dB.

The TD-SCDMA input-referred IP2 requirement is 20dBm, which can be satisfied without a calibration circuit. The layout of quadrature mixers is fully symmetric, and special attention is paid to the layout of the switching core. The minimum IIP2 of 25dBm is measured.

The receiver chain provides 62dB of voltage gain. Gain control is implemented in both the LNA and the analog filter section. The filter is an active-RC type, consisting of three stages. The first stage is a channel-select filter, which is 1st-order low-pass filter with a 3dB bandwidth of 310kHz. Since TD-SCDMA bandwidth is 1.28MHz, this filter distorts the received signal. To address this, it is calibrated within ±1% pole variation then compensated by the digital filter in ABB IC. Since the 1st-order filter cannot suppress the jammers completely, an ADC with dynamic range of 60dB is required in ABB IC so that the suppression can be carried out in the digital domain. Leveraging digital signal processing relaxes analog circuit design and reduces both power consumption and chip area. The 2nd-stage filter is the anti-alias filter for the ADC. The corner frequency is 4.5MHz. The last stage is the driving buffer, which has –3dB to 3dB voltage gain with 1dB gain step. The measured integrated receiver NF from 1kHz to 640kHz is 3.5dB (3.2dB) for 1900MHz (2010MHz) band.

The transmitter consists of a direct-upconversion modulator, a VGA, and a driver amplifier (DA). The modulator employs a traditional double-balanced mixer. This configuration suppresses the RF carrier and leaves the mismatch as the only source of the carrier leakage. Without employing the calibration techniques [2], the measured carrier suppression is 56dBc and the image rejection is 57dBc.

The required total gain control range of TD-SCDMA transmitter is 74dB, which is challenging. ABB IC provides 12dB of digital gain control and leave 62dB gain control in analog domain. To achieve this, two or more VGA stages are commonly utilized. Additional VGA stages degrade linearity performance and consume more power making the practice less favorable for achieving a high adjacent channel leakage ratio (ACLR). As illustrated in Fig. 19.5.2, the VGA employs a gain control circuit to achieve more than 40dB of gain control range. High and low gain switching is achieved by switching between G_{m1} (M_1, M_2, R_1) and G_{m2} (M_3, M_4, R_2). The fine gain step is realized by the switch transistor array. Two identical switching arrays are controlled by a pair of complimentary digital signals, one array is connected to V_{DD} and the other is connected to VGA output. As shown in Fig. 19.5.2, by turning on and off transistors K_1 to K_5, the gain can be stepped by 6dB. DA circuit also provides gain control. When the input is changed from G_{m3} (M_7, M_8) to G_{m4} (M_9, M_{10}), the gain of the DA is changed from high to low. The degeneration inductors L_3 and L_4 increase headroom and improve linearity. The measured gain control range for the VGA and DA combination is over 66dB, and the gain step is about 6dB. When the output power is 4.4dBm, the measured EVM is 3.7% and ACLR is –46 dBc as shown in Fig. 19.5.3, which are better than the TD-SCDMA system requirements.

The synthesizer is realized with a 3rd-order ΔΣ fractional-N PLL with a 26MHz external reference oscillator. The integrated VCO is designed to operate across both TD-SCDMA bands and is based on an LC resonant tank with a MOS diode varactor operating at twice the LO frequency. An array of multi-bit switch capacitors is used to ensure that the VCO tuning range is sufficient to cover both TD-SCDMA bands with production margin and to keep the VCO gain (K_{VCO}) low. The measured phase noise is –132dBc/Hz at 3.2MHz offset from a 1.9GHz carrier frequency. The integrated phase noise from 1kHz to 640kHz is about 0.85° as shown in Fig. 19.5.4. All reference and fractional spurs are at least 77dB below the carrier as demonstrated in Fig. 19.5.5. This level of spectral purity can be attributed to accurate matching between the UP and DOWN charge-pump currents, fully symmetric design and layout, lower VCO gain, and the use of dithering techniques for the ΔΣ block result

Rapid acquisition and settling is enabled through the VCO calibration algorithm which opens the loop at the beginning of the calibration cycle and selects the appropriate VCO operating band. Once the calibration is completed, the loop is closed and a high current auxiliary charge pump is enabled for a short period of time to increase the loop bandwidth and allow fast settling. The measured settling time is 70μs.

The key performance parameters of the transceiver are summarized in Fig. 19.5.6, which satisfies TD-SCDMA system requirement. Comparing to BiCMOS TD-SCDMA transceivers [3,4], it consumes about 30% less power from a 1.8V supply. A die micrograph is shown in Fig. 19.5.7 and its size is 2.8×2.8mm².

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[3] Maxim, MAX 2397 datasheet, http://www.maxim-ic.com/quick_view2.cfm/qv_pk/3860
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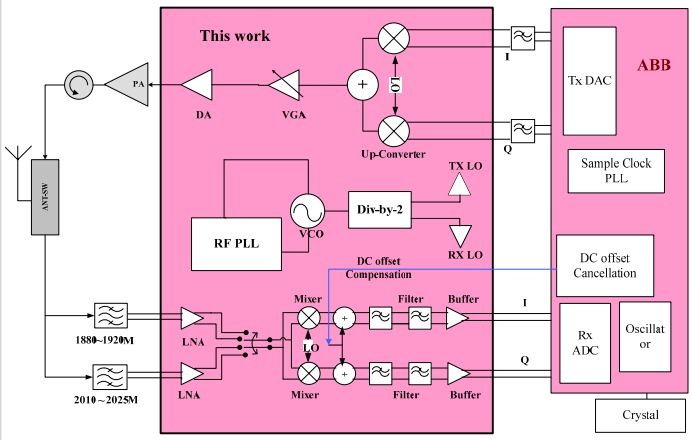

Figure 19.5.1: Dual-Band TD-SCDMA transceiver block diagram.

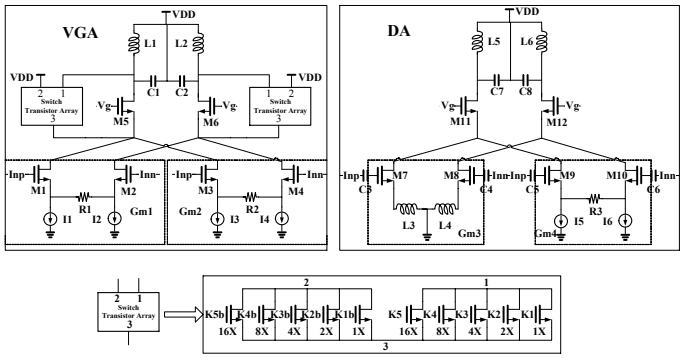

Figure 19.5.2: Schematic of the variable gain amplifier and the driver amplifier in the transmitter.

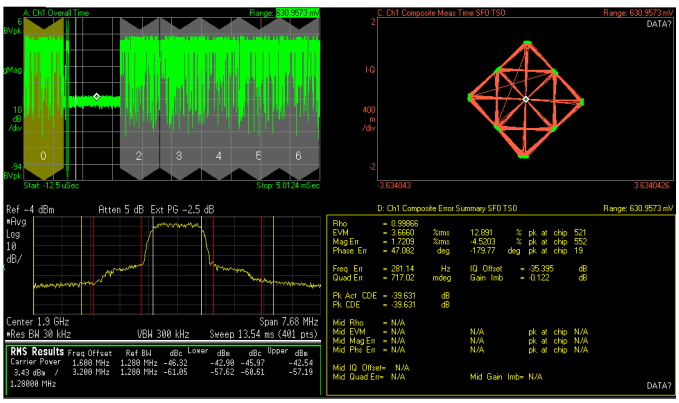

Figure 19.5.3: Measured transmitter EVM and ACLR, which are 3.7% and 46dBc, respectively.

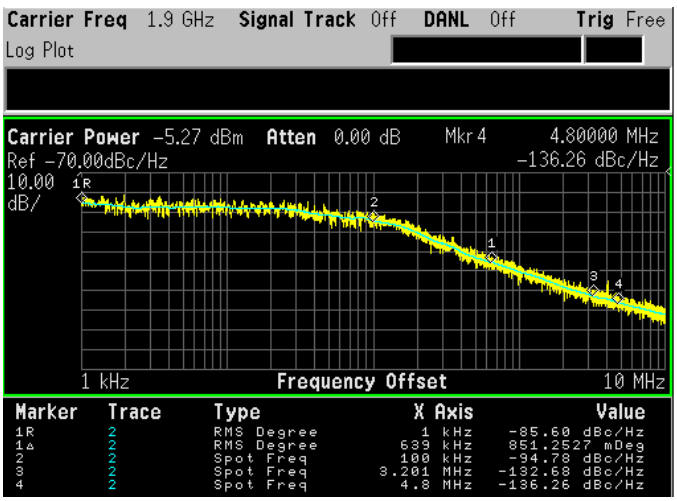

Figure 19.5.4: Measured synthesizer phase noise.

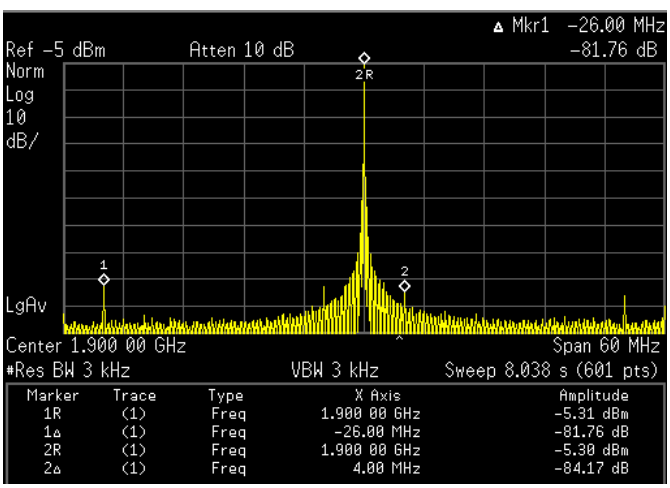

Figure 19.5.5: Measured reference spurs are 81dB below the carrier.

Parameter	Measured	Parameter	Measured
Frequency (MHz)	1880 to 1920, 2010 to 2025	**Transmitter**	
Receiver		Max. Output Power (dBm)	4.4
Noise Figure (dB)		P_{1dB} (dBm)	9
1880 to 1920MHz	3.5	Gain Control Range (dB)	66
2010 to 2025MHz	3.2	Gain Step (dB)	6
$\|S_{11}\|$ (dB)	<−11dB	Carrier Suppression (dBc)	56
IIP3 (dBm)	−14.5	Image Suppression (dBc)	57
IIP2 (dBm)	>25	ACLR (dBc) at 1.6 MHz	−46
Gain (dB)	62	EVM (%)	3.7
Power cons. (with PLL) (mW)	95	Power Cons. (with PLL) (mW)	158
Synthesizer			
Phase Noise (dBc/Hz): 3.2MHz offset 4.8MHz offset			−132 −136
Integrated Phase Error from 1kHz to 640kHz (degree rms)			0.85° rms
Discrete Spur (dBc): 10Hz to 4MHz >4 MHz			−77 −81
Lock Time (μs) (Includes VCO calibration and settling time)			70

Figure 19.5.6: Performance summary of the TD-SCDMA transceiver.

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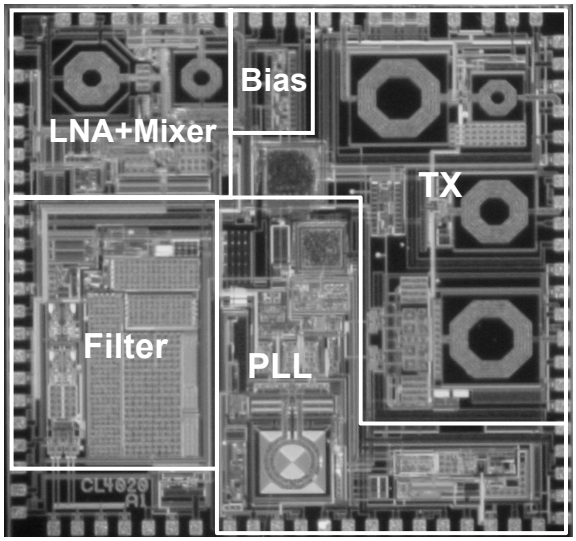

Figure 19.5.7: Single-chip dual-band TD-SCDMA transceiver die micrograph.

